

# PCI/Mini PCI/CardBus - AHB 33/66 MHz IP Core

## Features

- PCI 2.2-compliant, 32-bit, 33/66 MHz interface
- Mini PCI Specification revision 1.0 compliant
- CardBus compliant, 32-bit, 33MHz interface
- Conforms to AMBA AHB specification revision 2.0
- Compliant with PCI Bus Power Management Interface Specification revision 1.1
- Customizable, programmable, single-chip solution
- Predefined implementation for predictable timing
- Supports power management event
- Supported master functions:
  - memory read, memory write
  - interrupt acknowledge
  - parity generation / error detection
- Supported target functions:
  - zero wait state data transfer
  - type 0 configuration space header
  - medium decode speed
  - parity generation / error detection
  - configuration read, configuration write
  - memory read, memory write
  - target abort, target retry, target disconnect

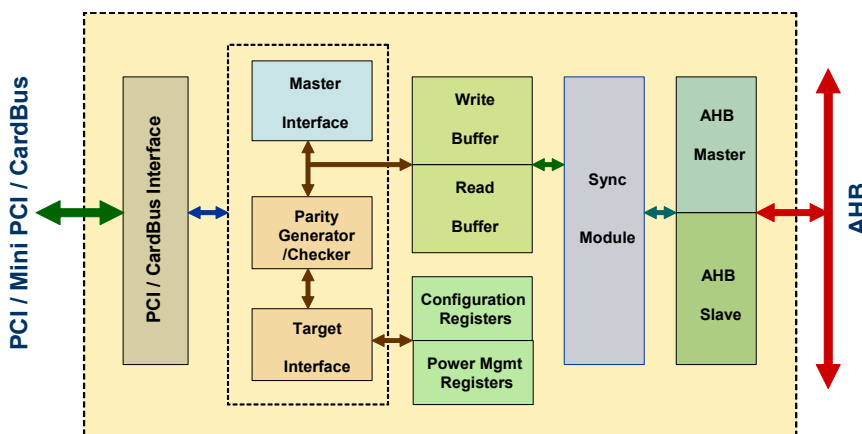
## Overview

The Arasan PCI/Mini PCI/CardBus - AHB IP Core is a 33/66 MHz high-performance PCI - AHB bridge, Mini PCI - AHB bridge, or CardBus - AHB bridge. The IP is compliant to PCI 2.2 and CardBus specifications. Applications of this IP core include Ethernet, wireless, USB, FireWire CardBus adapters, PCI add-on cards, PCMCIA adapter cards, and PCI - AHB bridges.

The PCI Local Bus is a high performance 32-bit bus with multiplexed address and data lines. The CardBus are PCMCIA 2.1 or later standards is also a 32-bit version of the PC Card. CardBus combines the low-power, small form-factor, hot insertion capability, and light weight of the PC Cards with the high-performance of the PCI. CardBus PC Cards support a maximum throughput of 132MB/second when operating with a Dword data bus. The CardBus cards, when inserted into a 68-pin CardBus socket, are automatically detected and configured by PCMCIA-specific software. The PCI/CardBus controller provides synchronous interface to the user applications. It acts both as a master and slave for corresponding AHB write and read transactions.

The AMBA AHB bus addresses the requirements of high-performance synthesizable design. It also supports multiple bus masters and provides high-bandwidth operation. The AHB bus supports burst transfer, split transactions, single-cycle bus master handover, single-clock edge operation, non-tristate implementation, and wider data bus configuration (64/128 bits).

PCI/Mini PCI/CardBus - AHB IP Core Functional Block Diagram



# PCI/Mini PCI/CardBus - AHB 33/66 MHz IP Core

## PCI/Mini PCI/CardBus Interface:

The PCI/Mini PCI/CardBus bus interface provides a synchronous interface during both the master and target mode of operations. The PCI/Mini PCI/CardBus Bus Interface unit provides the interface for the master, target, and parity generator/checker functional blocks. It also supports power management functions.

## Parity Generator/Checker:

This block calculates parity of the address and command/byte enables. The parity is placed on the PCI bus during read and write transactions. The Parity Generator/Checker checks the correctness of parity over address and command/byte enables received during target write and data phase of master read transaction. It also updates Status register bits based on the address and data parity calculations.

## AHB/APB Interface:

The AHB master is responsible for transferring data between the ARM processor and

PCI/Mini PCI/CardBus-AHB bridge for read and writes operations. AHB slave block houses the Operational registers. It handles reading and writing of these registers by both PCI/Mini PCI/CardBus-AHB bridge and ARM processor.

## Synchronization module:

This block has handshake logic to communicate with the BIU on one side and the AHB master and slave on the other side. The FIFO size is parameterizable. It has a minimum size of one DWORD and is expandable to a size that fits user's specific applications.

The Arasan PCI/Mini PCI/CardBus - AHB IP Core is an RTL design in Verilog and VHDL that implements a PCI/Mini PCI/CardBus - AHB bridge on an ASIC, or FPGA. The core includes RTL code, test scripts and a test environment for full simulation verifications. The Arasan PCI/Mini PCI/CardBus - AHB IP Core has been widely used in different PCI/Mini PCI/CardBus applications by major chip vendors.

## Benefits:

- Fully compliant core with proven silicon
- Premier direct support from Arasan IP core designers
- Easy-to-use industry standard test environment
- Unencrypted source code allows easy implementation
- ReUse Methodology Manual guidelines (RMM) compliant verilog code ensured using Spyglass

## Deliverables:

- RMM Compliant Synthesizable RTL design in Verilog
- Easy-to-use test environment
- Synthesis scripts
- Technical documents

## Supported Platforms/Simulators:

- Platforms: Solaris, Unix, Linux and Win XP
- Verilog simulators: Synopsys VCS, Cadence NC-Verilog, MTI ModelSim-Verilog

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## Data Sheet Links:

PCI/Mini PCI/CardBus - AHB IP Core:  
<http://www.arasan.com/datasheets/login.php>

For a complete directory of Arasan IPs, please visit:  
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