

Features

- **General**
 - Compliant to ONFI 2.2 standard
 - Supports Flash devices up to 128Gb
 - Supports NAND Flash memories from Micron, Samsung, ST-Micro and others.
 - Boot mode support
 - Supports all mandatory commands and selected optional commands
 - Supports interleaved reads for better performance
 - Supports small data movement
 - Full access to spare area
- **Configuration**
 - Page Size - 512B, 2KB, 4KB
 - Bank/chip select options
 - Programmable timing
 - Address cycles - 4, 5
 - ECC - enable, disable
 - Flash data bus width - 8bit or 16bit
 - RAM size
- **ECC**
 - MLC - BCH
 - Configurable Block size (512B, 1KB, 2KB)
 - Standard support: 4,8,12 bit error correction for 512B (max upto 32 bit error correction)
 - Additional support of software configurability for the error correction
- **Data Interface**
 - Bandwidth 166 MBps [Sync mode 4] and 200 MBps [Sync mode 5]
 - Supports asynchronous modes [0-5]
 - Supports synchronous modes
 - 8/16 bit data bus width
 - Supports independent data bus
- **System Interface**
 - AHB - AMBA 2.0 Compliant
 - APB - AMBA 2.0 Compliant
 - PIO Mode
 - Slave DMA mode

NAND Flash Controller IP Core

MLC Flash Memory

Overview

The NAND Flash landscape is changing and the Arasan NAND Flash Controller IP Core is changing with it. New applications are emerging, and innovative IP solutions are needed to keep pace. NAND Flash is being incorporated into all types of products including portable memory drives, media players, digital cameras, PDAs, digital TVs, digital camcorders, PCs, etc. And Arasan is in the perfect position to give you what you need.

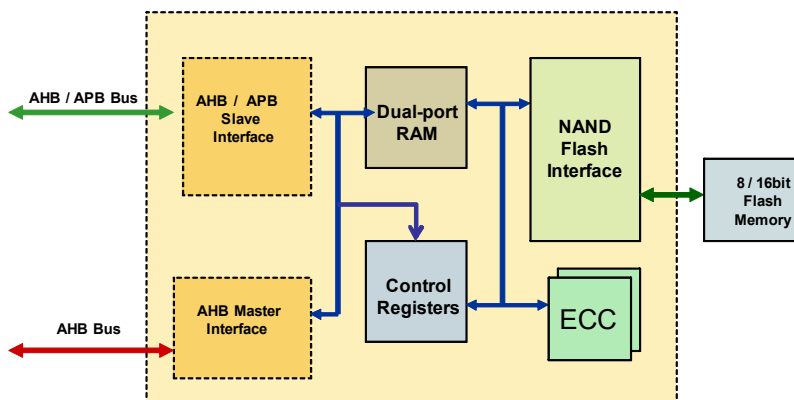
The Arasan NAND Flash Controller IP Core is a full featured, easy to use, synthesizable core, easily integrated into a SoC or FPGA. Designed to support MLC flash memories, it is flexible in use and easy in implementation. The controller works with any suitable memory device up to 128 Gb from leading memory providers such as Micron, Samsung, Toshiba, Hynix, ST-Micro, and others. The IP core includes a host of configuration options from page size to band selects. The controller uses BCH (option for 4-, 8-, up to 32 bit error correction) based Error Code Correction (ECC) for optimized performance and reliability. Additional features include the capability to boot from flash.

The IP core supports the Open NAND Flash Interface Working Group (ONFI) 2.2 standard. It also supports a variety of host bus interfaces for easy integration into any design architecture - AHB, APB, OCP, 8051, or custom buses. The slave AHB IP supports an external DMA interface whereas the master AHB IP incorporates an internal DMA controller.

An optional NAND Flash File system is available to support advanced features. The file system converts complicated tasks of NAND flash memory interfacing to simple memory access. Flash memory read, write, garbage collection, bad block management, and other functions are handled in the background by the file system.

Arasan provides a "Total IP Solution" for its NAND Flash Controller IP Core. These cores are fully tested with vendor memory models. The collateral for this IP core consists of RTL code, EDA scripts, test environment and documentation, all backed by Arasan's World-class customer support.

NAND Flash Controller IP Core Functional Block Diagram



NAND Flash Controller IP Core

NAND Flash Interface:

The NAND Flash Interface handles all the command, address, and data sequences and manages all the hardware protocols. It is ONFI 2.2 compliant and provides an 8-bit or 16-bit interface to the flash memories. The interface supports a maximum of 128Gb of NAND flash memory. Both source synchronous and asynchronous data interfaces are supported. All timing modes (0-5) are supported for the asynchronous mode. Timing mode0 is also supported for the source synchronous mode.

AHB/APB Interface:

The AHB/APB master/slave block consists of the operational registers. A processor connecting to the custom interface can control the operation of the NAND Flash controller through the NAND Flash control registers. Read/write operations of the flash memory can be performed through the DPRAM or NAND flash interface. The AHB/APB master interface can be used to transfer boot code from the NAND flash memory to the system memory during system power-up.

Host Interface:

A custom host interface can be chosen to provide a mass storage capacity of up to 128 Gb. The custom interface includes the AHB, APB, OCP, SD, PC Card, CardBus, CompactFlash, Avalon, BVCI, generic parallel, 8051, and custom buses. A host connecting to the custom interface controls the operation of the NAND Flash Controller through the NAND Flash Control Registers. Read/write operations of the flash memory can be performed through the DPRAM or NAND flash interface.

Control Registers:

The host processor controls the configuration and operation of the NAND Flash Controller through the Control Registers. Configuration includes the setting of hold time, setup time, wait state, memory configuration, timing modes, etc. The Control Registers also provide operating status such as Busy and Data Ready signals.

NAND Flash File system:

NAND Flash file system is available as an option to the NAND Flash IP core. Designed specifically to work with the Arasan NAND Flash IP, it is optimized to support key features of the IP core. Designed with the Linux operating system, it can be easily ported to a variety of other operating systems to fit any application.

ECC:

The ECC module provides error detection and correction support for MLC Flash memory. The BCH Code supports the MLC Flash memory, providing up to 32 bit error correction. An additional pipeline stage in the BCH decoder can be enabled to maximum performance. The number of error bits to be corrected can be set via a software interface.

Benefits:

- Fully compliant core with proven silicon
- Premier direct support from Arasan IP core designers
- Easy-to-use industry standard test environment
- Unencrypted source code allows easy implementation
- ReUse Methodology Manual guidelines (RMM) compliant verilog code ensured using Spy-glass

Deliverables:

- RMM Compliant Synthesizable RTL design in Verilog
- Easy-to-use test environment
- Synthesis scripts
- Technical documents

Supported Platforms/Simulators:

- Platforms: Solaris, Unix, Linux, WinCE, and Win XP
- Verilog simulators: Synopsys VCS, Cadence NC-Verilog, MTI ModelSim-Verilog

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Data Sheet Links:

NAND Flash Controller IP Core Data Sheet:
<http://www.arasan.com/datasheets/login.php>

For a complete directory of Arasan IPs, please visit:
www.arasan.com

