

MIPI® Solutions

- IP Collateral
 - IP Cores
 - PHYs
 - vIP Validation
 - Software Stacks
 - Protocol Analyzers

- Intellectual Property - IP Cores
 - UniProSM v1.1
 - SLIMbus® Host & Device v1.0
 - CSI-2 Transmit & Receive v1.0
 - DSI Host & Device v1.01
 - DigRFSM v3.09.04
 - DigRFSM v4
 - HSI v1.0
 - D-PHY v1.0
 - M-PHYSM *

- Verification IP - VIP
 - Integrated into IP offering

- Protocol Analyzer
 - SLIMbus®

- Software Stacks
 - UniPro
 - SLIMbus
 - HSI

- System Interface Options
 - AHB - AMBA 2.0
 - APB - AMBA 2.0
 - OCP 2.0
 - AXI
 - Custom Interfaces

- End Products
 - Smart Phones
 - Netbooks
 - Set Top Boxes
 - Game consoles

* Draft Specification

MIPI® Solutions

Overview

Arasan is a leading provider of MIPI® interface IP and has the most comprehensive IP portfolio in the market today. Arasan has been an Executive Member of the MIPI® Alliance since 2004 and has licensed its IP to leading Tier 1 OEMs.

With the rising demand for feature rich mobile platforms such as smartphones and netbooks, system and SoC designers need a stable set of interface IP that can integrate the multitude of features in these platforms. The MIPI family of interfaces meet these objectives and simplify mobile platform design. SoC designers are assured of the highest quality of MIPI IP cores from Arasan - enabling them to reduce implementation risk and speed up product development. Arasan provides a “Total IP Solution” for MIPI IP comprising of IP cores, verification IP, software stacks and protocol analyzers.

Arasan Intellectual Property (IP) Cores:

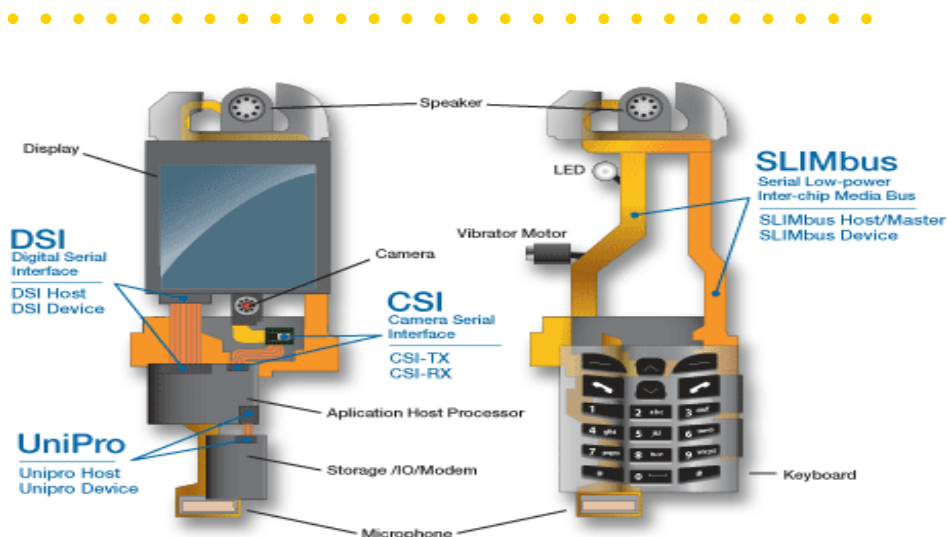
Our portfolio consists of all of the major interfaces of MIPI. Arasan has developed deep domain expertise in MIPI protocols, leading to the development of high quality, compliant IP cores. By leveraging Arasan’s MIPI IP cores, system companies can quickly bring innovative, feature rich solutions to the market with minimal risk.

Arasan Verification IP (VIP) Cores:

In addition to providing the IP cores, Arasan provides a verification IP and test environment to allow comprehensive verification, validation, debugging and testing of the system. The test environment captures our MIPI interface expertise and enables customers to rapidly develop their test environment.

Arasan Software Stacks:

Complementing its offering of MIPI IP, Arasan offers Software Stacks that ease the system-level integration and development of MIPI based mobile platforms. These highly portable stacks can be quickly adapted to a specific processor and OS platform.



MIPI Solution

UniProSM

Arasan's UniPro controller is compliant with UniPro v1.1 specification and can scale to support multiple data lanes. It has a standard PPI interface to a D-PHY (also available from Arasan). The UniPro IP core integrates all layers defined by UniPro specification. A software stack is also available from Arasan.

SLIMbus[®]

Our portfolio includes both Host and Device IP cores and the corresponding software stack. Compliant with the latest 1.0 specification, SLIMbus is a multi-drop, two-wire interface which replaces a number of proprietary control and audio buses, relieving PCB routing in cramped mobile platforms. The IP supports clock gearing to reduce power and is able to support data traffic with differing bandwidth requirements.

CSI-2

CSI-2 interfaces are used to connect an application processor with a camera module. Its high-bandwidth serial interface can scale to support high resolution image sensors becoming more prevalent in the market today. Arasan's CSI-2 IP cores are available in both transmit and receive configurations and interface with our D-PHY over a standard PPI interface. The IP is compliant with CSI-2 v1.0 specification.

DSI

Arasan's DSI IP core is compliant with v1.01 specification and offers both host and device configurations to connect a display module with an application processor. As the resolution and color depth of mobile displays scale, a DSI based interface simplifies system design by replacing prior generation of parallel bus with a high-performance serial interface.

DigRFSM

The rapid deployment of 2.5G and 3G networks has led to the development of custom RF chips to support these new cellular standards. DigRF is a standard interface to connect such chips with a baseband/application processor. Arasan's IP is compliant with the latest specification v3.09.04.

HSI

Realizing the need for development of System-in-Package (SiP) solutions for the ever decreasing form-factor of mobile platforms, the HSI interface is optimized for die level interconnect. Arasan's HSI IP core is compliant with the latest v1.0 specification and supports full-duplex traffic. A software stack is also available.

D-PHY

The benefit of MIPI interfaces is their low power, low pin-count yet being able to support high bandwidth transfers. This is achieved by using a dedicated D-PHY. Arasan has developed D-PHY macros that are compliant with the latest v1.0 standard. It can be ported to other processes and foundries as well as customized for specific applications. The D-PHY supports a High-Speed (HS) mode for fast data transfers and a Low Power (LP) mode for control transactions.

SLIMbus[®] Analyzer

The SLIMbus analyzer developed by Arasan is a versatile tool to assist in the development and debug of SLIMbus systems. The analyzer is bundled with an intuitive GUI that allows the user to capture, process and filter SLIMbus traffic for debugging.

Benefits:

- Fully compliant core with proven silicon
- Premier direct support from Arasan IP core designers
- Easy-to-use industry standard test environment
- Unencrypted source code allows easy implementation
- ReUse Methodology Manual guidelines (RMM) compliant verilog code ensured using Spy-glass

Deliverables:

- RMM Compliant Synthesizable RTL design in Verilog
- Easy-to-use test environment
- Synthesis scripts
- Technical documents

Supported Platforms/Simulators:

- Platforms: Solaris, Unix, Linux, WinCE, and Win XP
- Verilog simulators: Synopsys VCS, Cadence NC-Verilog, MTI ModelSim-Verilog

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Data Sheet Links:

MIPI Solutions Data Sheet:
<http://www.arasan.com/products>

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