

## Features

### Verilog Test Environment

- Functional verification, validation, and compliance testing
- DSI Host BFM, DSI Device BFM and D-PHY BFM
- User-friendly monitor

### Verification Test Conformance

- Display Serial Interface (DSI) v1.01.00
- Display Pixel Interface (DPI-2) v2.00
- Display Bus Interface (DBI-2) v2.00
- Display Command Set (DCS) v1.02
- MIPI D-PHY v0.92

### Clock/Data Signaling

- One to four PHY data lanes
- One clock lane
- High-speed and low-power modes
- HS mode: 80-1000 Mb/s sync transfer
- Differential signaling for HS data
- LP mode: 10 Mb/s async transfer
- Spaced one hot encoding for LP data
- Ultra low power, escape, high speed, and control modes
- Switching to ultra low power mode during shutdown
- Contention recovery mechanism
- Bus turnaround
- Injection and detection of error conditions

### Display format and mode support

- Command and Video modes
- Type 1, 2, 3, and 4 display architectures
- 16bpp RGB565, 18bpp RGB666, and 24bpp RGB888 pixel formats
- QQVGA, OCIF, QVGA, CIF, VGA, WVGA, and XVGA resolutions
- Video mode streaming in non-burst mode with sync pulses or sync events and burst modes
- Multiple high-speed packets per transmission
- Acknowledge packets and trigger messages
- Interleaved data streams
- Reverse LPDT transmission and reception
- DCS generic read/write packets
- Null and blanking packets
- EOT packet enabling/disabling feature for backward compatibility
- Tearing effect

# DSI Verification IP

## Overview

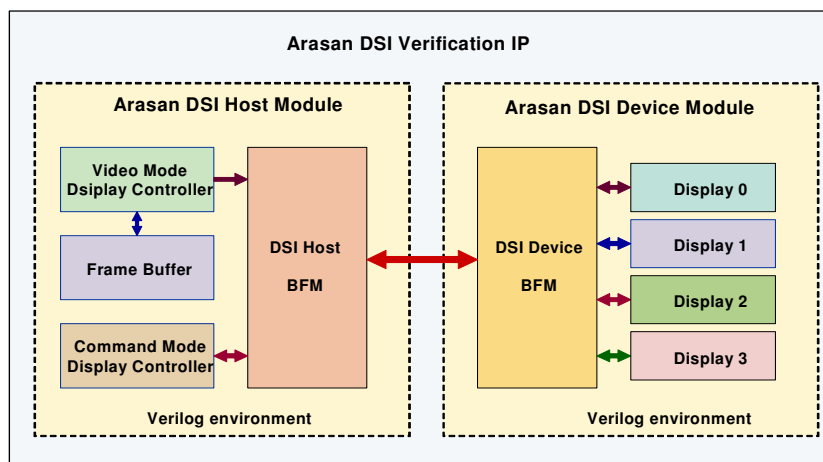
The Arasan DSI Verification IP is a comprehensive test environment for verification, validation, debugging, and testing of MIPI DSI (Display Serial Interface) applications for functionality, compliance, or interoperability. The DSI Verification IP allows the complete and extensive testing of DSI applications, it also ensures full functionality of the SoC or ASIC before the design is finalized. The MIPI compliant DSI Verification IP is delivered with an interconnected host and device test environment, the same setup supports the verification and testing of MIPI DSI device IPs as well as MIPI DSI host IPs.

The Arasan DSI Verification IP includes a DSI Host module, a DSI Device module, and a D-PHY transceiver module. The DSI Host module consists of the DSI Host controller behavior functional model (BFM), Command File, Input Data File, Output Data File, and Monitor. The Command File provides a comprehensive set of test vectors as well as a complete set of MIPI DSI compliant commands for extensive testing. A Verilog test environment can be setup easily by replacing the DSI IP of the DSI Verification IP with the application IP or device under test (DUT), no interconnection on the DSI bus is required. The DSI Device module consists of components similar to that of the DSI Host module. For applications written in VHDL, a mixed test environment can be employed.

The DSI Verification IP also allows the injection and detection of errors and exception conditions. These error conditions include CRC, ECC, time-out, invalid commands, and protocol errors.

The DSI Verification IP supports video mode, command mode, major pixel formats, burst mode, non-burst mode, and virtual channels.

## Arasan DSI Verification IP



# DSI Verification IP

## DSI Host BFM:

The DSI Host BFM consists of the DSI protocol layer and PPI\_PHY layer. The DSI protocol layer is responsible for the DSI specific functionality, and the PHY layer is responsible for the PHY functionality. The DSI host model reads commands from a command file. Based on the tasks listed in the command file, pixel data is generated from the respective data files. If the command is of the type “long packet”, each long packet will consist of a packet header along with the supplied parameters like word count, data identifier, virtual channel number, ECC, payload data, and CRC.

Since both layers are supported, PHY layer commands can be issued to change the DSI controller operating mode to ultra low power mode, low power mode, or bus turnaround.

## DSI Device BFM:

The DSI Device BFM handles the DSI receiver protocol and PHY specific protocol. De-packetization is carried out by this model based on the accompanied packet headers or data identifier types. Received payload data is sent to respective data collector files. The

packet reception sequence is listed in a packet data file. Based on the specified virtual channel, the packet is routed to different display panel. Trigger messages, short packets or long packets can also be sent by the receiver during bus turn around. Data needed to be packed at low power mode is fetched from a data sending file. Contention on the DSI traffic can also be forced using this model.

## PHY Transceiver Model:

The D-PHY model emulates the functionality of a D-PHY transceiver.

The model drives the differential signals at high-speed during transmission. It combines the multi-lane signals into a single stream during reception.

This D-PHY model also handles low power single ended signals during reception and transmission.

## Benefits:

- Fully compliant core
- Premier direct support from Arasan VIP core designers
- Easy-to-use industry standard test environment
- Unencrypted source code allows easy implementation

## Deliverables:

- Perl script for regression testing
- Standalone test environment
- Test environment documentation
- Test cases

## Supported Platforms/Simulators:

- Platforms: Linux and Win XP
- Verilog simulators: Synopsys VCS, Cadence NC-Verilog, MTI ModelSim-Verilog



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## Data Sheet Links:

DSI Verification IP:  
<http://www.arasan.com/datasheets/login.php>

For a complete directory of Arasan IPs, please visit:  
[www.arasan.com](http://www.arasan.com)