

Features

- Compliance
 - xD Picture Card Host Guideline v1.2
 - xD Picture Card Specification v1.2

- IP Detail
 - Async: 8 bit data mode
 - I/O: 8 bit data mode
 - Supports all variants standard, M, H
 - Up to 2 GB capacity
 - Comfortable erase mechanism
 - Supports Master Mode operation
 - Programmable Access Timing
 - Supports Slave DMA Page Read, Write operations
 - Supports ECC generation and checking
 - Multi-block programming and erase

- End Products
 - Picture Frames
 - Digital Camera
 - Smart Phones
 - Game Systems
 - Laptops
 - Printers

xD Host Controller IP

Overview

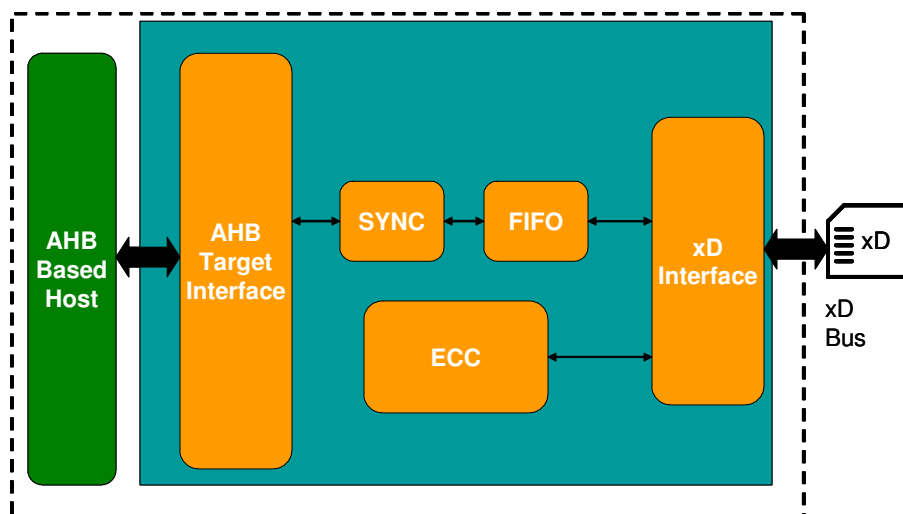
As the mobile industry continues to grow, the requirements for both internal and external memory are increasing at an exponential rate. At the system level, memory interfaces with larger capacities, smaller form factor and faster access times in addition to support for multiple industry standards are needed.

Arasan Chip System's xD Host Controller IP is a highly integrated solution that is compliant with the xD Picture Host Guideline v1.2 and Card v1.2 specification. The controller handles all of the command, address and data sequences to manage the xD protocol. In addition it performs ECC generation and checking for xD. A host can access and configure this IP using the standard AHB bus interface.

The host controller access data in the xD card using simple register accesses as the controller takes care of the timing and ECC specified by xD standard.

In addition to providing the xD Controller IP core, Arasan provides a complete verification and test environment as well as bus functional models to ease integration of thus IP into an SoC.

xD Host Controller Functional Block Diagram



xD Host Controller IP

xD Picture Card

Arasan's xD (Xtreme Digital) Picture controller is fully compliant with xD specification 1.2. The controller enables a high-speed, low-power data storage access primarily for digital cameras. It includes key features such as programmable access timing and ECC detection and correction.

AHB System Interface

The default system bus interface is an AHB interface. The AHB slave interface is used to access registers to configure the IP. The AHB master interface is used for data transfer between the host system and the FIFO internal to the IP. A slave DMA function is implemented which enables efficient data transfer while minimizing the load on the host cpu.

SYNC

This block has handshake logic to coordinate the timing and transfer of data

between the AHB bus and the data on the xD interface.

ECC

The logic in this block handles both ECC detection and correction for the xD protocol. The calculated value of ECC is placed in the ECC field during xD card writes. On receipt of data, the ECC block re-calculates it and compares it to the stored value for error detection. Single bit errors are corrected by this logic.

FIFO

The FIFO is used to buffer data so as enable the host to operate independently from the xD Interface block.

xD Interface

This block handles all of the command, address, data sequences and manages the hardware protocol of the xD standard. This block simplifies the host access to the xD data.

Benefits:

- Fully compliant core with proven silicon
- Premier direct support from Arasan IP core designers
- Easy-to-use industry standard test environment
- Unencrypted source code allows easy implementation
- Reuse Methodology Manual guidelines (RMM) compliant verilog code ensured using Spy-glass

Deliverables:

- RMM Compliant Synthesizable RTL design in Verilog
- Easy-to-use test environment
- Synthesis scripts
- Technical documents

Supported Platforms/Simulators:

- Platforms: Unix, Linux, Win XP
- Verilog simulators: Synopsys VCS, Cadence NC-Verilog, MTI ModelSim-Verilog

Application Examples



Arasan Chip Systems, Inc.

2010 N. First St. Suite #510
San Jose CA 95131
Phone: 408-282-1600
Fax: 408-282-7800
E-mail: sales@arasan.com

Data Sheet Links:

xD Host Controller IP Data Sheet:
<http://www.arasan.com/datasheets/login.php>

For a complete directory of Arasan IPs, please visit:
www.arasan.com