

Features

MMC 4.4 (eMMC)

- Complies to MultiMedia Card System Specification Version 4.4 (eMMC)
- Peak bandwidth of 104MBps with Dual-data rate
- Supports 1-, 4-, or 8-bit data bus
- Dedicated Hardware reset pin (RST_n)
- Compatibility with previous MMC standards
- Supports over 2GB memory capacity
- Multiple boot modes - Power-on, Alternate boot mode
- Supports multiple Partition Management features with enhanced storage options
- Sector address allows host to access high capacity card
- New security features such as secure erase, Replay Protected Memory Block (RPMB)
- Sleep mode for power saving
- CID register to recognize eMMC or card
- CRC7 for command and CRC16 for data integrity
- Card write protection (power on, temporary and permanent) and password features
- Performs Secure Erase, Secure TRIM and TRIM operations
- Supports block lengths or sector sizes of 512, 1024, and 2048 bytes

AHB

- Complies to AMBA specification version 2.0.
- Supports incremental burst transfers in DMA mode
- Supports register transfer in non-DMA mode
- Supports retry and split

MMC/eMMC 4.4 Memory Controller IP

Overview

MMC/eMMC 4.4 is the latest specification released by JEDEC and is designed to meet the requirements for secure yet flexible program code and user data storage for emerging consumer electronic products. With its low-pin count, high bandwidth and multiple boot mechanisms MMC/eMMC 4.4 greatly simplifies the system design for these new products.

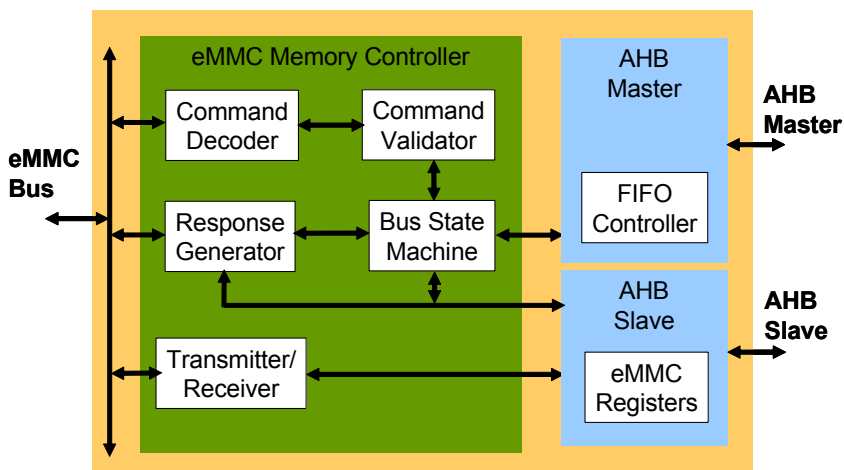
Arasan's MMC/eMMC 4.4 Memory Controller IP is compliant with the MMC 4.4 (eMMC) standard. The controller provides a bandwidth of 104MB/s when operating in DDR mode. A NAND flash memory device can be connected to the MMC/eMMC Memory controller. In such an implementation, the controller's AHB interface provides a channel for data transfers between the MMC/eMMC Memory Controller and a NAND flash controller (also available from Arasan). The Memory Controller supports the newer eMMC functions such as multiple boot partitions, flexible card data partitions, replay protected memory block and secure erase.

The MMC/eMMC Memory Controller is designed to operate at a maximum frequency of 52 MHz. The interface supports MMC 1-bit, 4-bit, and 8-bit modes. eMMC supports power-on booting without the upper level of software driver which simplifies system design. The controller shields the host system from the functional differences amongst various NAND flash architectures (such as MLC). The explicit sleep mode allows the host to instruct the controller to directly enter a low power sleep mode. The controller supports block lengths or sector sizes of 512, 1024 and 2048 bytes.

Arasan provides a "Total IP Solution" for the MMC/eMMC Memory Controller. The collateral provided includes RTL source files suitable for ASIC or FPGA implementation, synthesis scripts, test environment all backed by Arasan's World-class customer support.



MMC/eMMC Memory Controller IP Core Functional Block Diagram



MMC/eMMC 4.4 Memory Controller IP

MMC/eMMC Memory Controller:

The Memory Controller comprises of the Command Decoder, Command Validator, Response Generator, Receiver, Transmitter, and Bus State Machine. The Command Decoder registers the 48-bit command for all modes including MMC 1-bit, 4-bit, and 8-bit modes. It also verifies the CRC of the received commands. The Response Generator sends appropriate responses for the commands in all modes. The Transmitter and Receiver handles data transactions in all modes. Abort protocol is supported. The Command Validator validates received commands based on the state of the controller. This block checks for parameter errors, address errors and all errors in the argument field of the command. It also handles password authentications and is responsible to check if the card is locked or unlocked. The Bus State Machine handles the bus states as described in the MMC/eMMC card specification. The MMC/eMMC compliant controller supports additional features such as power-on

boot, alternate boot, replay protected memory block, sleep mode, and sector address mapping for high-capacity card access.

AHB/APB Interface:

The AHB interface consists of the master interface and slave interface. The AHB slave is used by external processor to configure the MMC/eMMC Memory controller, and for programming the control of data transfer between the controller and application's memory. The AHB master interface is used to transfer packets between the internal FIFOs and application memory. Before an AMBA AHB transfer can commence, the bus master must be granted access to the bus. This process is initiated by the master asserting a request signal to the arbiter. Then the arbiter indicates when the master will be granted the use of the bus. A granted bus master starts an AHB transfer by driving the address and control signals.

Benefits:

- Fully compliant core
- Premier direct support from Arasan IP core designers
- Easy-to-use industry standard test environment
- Reuse Methodology Manual guidelines (RMM) compliant verilog code

Deliverables:

- RMM Compliant Synthesizable RTL design in Verilog
- Easy-to-use test environment
- Synthesis scripts
- Technical documents



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