Arasan
The Bus Stops Here

PRODUCT OVERVIEW

CF+ / xD Host Controller IP

Features

- Memory Card Formats
  - CF+ 4.1
  - xD 1.2
- IP Details
  - Supports two slots
  - CF+ - Compact Flash
    - Memory: 8, 16 bit data mode
    - I/O: 8, 16 bit data mode
    - TrueIDE: 16 bit data mode
  - xD - Extreme Digital
    - Async: 8 bit data mode
    - I/O: 8 bit data mode
  - Built-in support for slave DMA
- End Products
  - SSD - Solid State Drives
  - Picture frames
  - Laptops
  - Printers
  - Digital Cameras
  - Smart Phones
  - Games Consoles

Overview

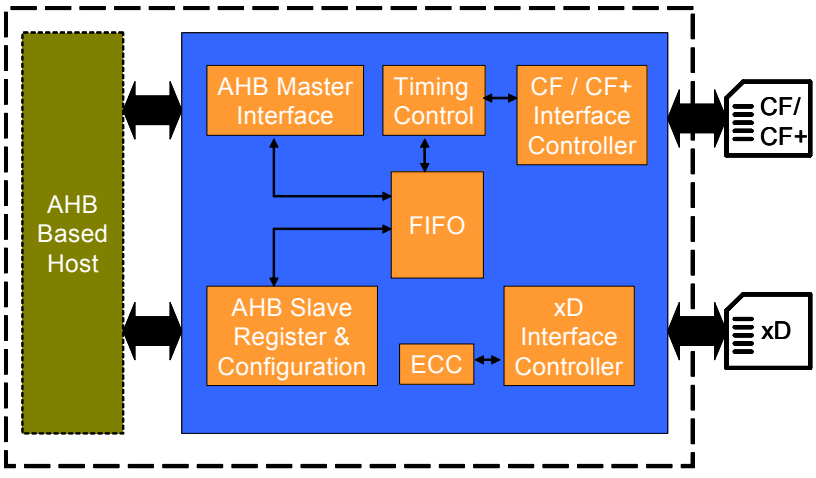
As the mobile industry continues to grow, the requirements for both internal and external memory are increasing at an exponential rate. At the system level, memory interfaces with larger capacities, smaller form factor and faster access times in addition to support for multiple industry standards are needed.

Arasan Chip System's CF+ / xD IP is a highly integrated host controller IP solution that supports two key memory and I/O technologies. Arasan's IP supports all timings and access methods (PC card memory, I/O and true IDE) specified in the CF+ standard. In addition it performs ECC generation and checking for xD. A host can access and configure this IP using the standard AHB bus interface.

The CF/CF+ Interface block in IP handles memory, I/O, true IDE transfers based on instructions from the host. It gets the timing information from the Timing Controller block and uses this timing information to perform the data transfer. The xD Interface block handles all the command, address, data sequences to manage the xD hardware protocols. Multi-block writes and erase accesses are supported to further improve performance. The host processor controls the configuration and operation of the controller through the AHB slave interface. Typical configuration settings includes timing modes, transaction types and data transfer modes.

In addition to providing the CD+ / xD IP core, Arasan provides a verification IP and test environment to ease integration into an SoC.

CF+ / xD Host IP Block Diagram



CF+ / xD Host Controller IP

CF+ / xD Controller

The Arasan CF+ / xD IP core is an integration of key industry memory and storage specifications into a single solution. Optimized for size and performance, it shares common functional blocks to minimize the size implementation. Similar to the family of memory controllers, it can support embedded or two external slots. A variety of host interfaces can also be supported. The IP supports CF/CF+ and the xD card formats.

CF/CF+

Arasan's CF/CF+ (CompactFlash) controller is fully compliant with CF card specification 4.1, PC Card 8.0, PCMCIA 2.1/JIEDA 4.2, and ATA/ATA-6 and is highly optimized to support three basic modes of operation: a) PC Card I/O mode, b) PC card Memory Mode and c) True IDE Mode. It supports an 8 or 16 bit data interface and implements a flexible scatter-gather DMA for data transfers. It also supports PIO mode and Ultra DMA for enhanced system performance. An independent clocking structure provides additional design flexibility and is optimized for system performance.

xD Picture Card

Arasan's xD (Xtreme Digital) Picture controller is fully compliant with xD specification 1.2. The controller enables a high-speed, low-power data storage access primarily for digital cameras. It includes key features such as programmable access timing and ECC detection and correction.

Target Applications

Primarily focused on mobile applications requiring memory controllers such as smartphones and similar application-rich systems, Arasan's CF+ / xD IP is also applicable to product categories such as picture frames, cameras, printers, MIDs, UMDs, PDAs and other consumer electronics.

Various Multi-Card Applications

Benefits:

- Fully compliant core with proven silicon
- Premier direct support from Arasan IP core designers
- Easy-to-use industry standard test environment
- Unencrypted source code allows easy implementation
- Reuse Methodology Manual guidelines (RMM) compliant verilog code ensured using Spyglass

Deliverables:

- RMM Compliant Synthesizable RTL design in Verilog
- Easy-to-use test environment
- Synthesis scripts
- Technical documents

Supported Platforms/Simulators:

- Platforms: Solaris, Unix, Linux, WinCE, and Win XP
- Verilog simulators: Synopsys VCS, Cadence NC-Verilog, MTI ModelSim-Verilog

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Data Sheet Links:

Memory & Storage IP Core data sheet:
http://www.arasan.com/datasheets/login.php

For a complete directory of Arasan IPs, please visit:
www.arasan.com