

## Features

### General Functions:

- Hardware Assisted 1588 V1/V2 Support
- Full-duplex mode at 10/100/1000 Mbps
- Half-duplex mode at 10/100 Mbps
- Supports IEEE 802.3-2002 compliant MII, RMII, SMII, GMII, RGMII, and SGMII
- Independent 32-bit scatter-gather DMA with big/little endian operation
- Optional VLAN Q-Tag frame support
- CSMA/CD Protocol for half-duplex mode
- PAUSE frame based flow control in full-duplex mode
- MDIO/MDC management interface
- 802.3 compliant MIB, SNMP, RMON management support
- Configurable transmit and receive FIFOs
- Supports Jumbo frames
- Supports magic packet and Wake-Up frames
- Optional AXI, AHB, PCIe, PCI or custom bus interface

### Transmit Functions:

- Variable length Inter Frame Gap (IFG) on back to back frame transmission
- Variable length (3, 5, 7 bytes) preamble generation
- Automatic generation of FCS and PAD
- Option to disable PAD or CRC32
- Option to stop frame retransmission on collisions
- TimeStamps the specified PTP Packets for implementing 1588 Protocol.

### Receive Functions:

- Inter Frame Gap checking
- Preamble detection and stripping
- Flexible address filtering modes and inverse address filtering
- 64-bit hash table to filter multicast addresses
- Promiscuous mode of operation
- Reception of broadcast frames
- Automatic checking the FCS field, runt frames, and data field length
- Detection of MaxFrameLen frames, receive errors
- 32-bit status information on each receive frame
- Identifies PTP Frames (both V1 and/or V2) in L2/L4 Encapsulation and TimeStamps for implementing 1588 Protocol.

### Flow Control Functions:

- Software controlled PAUSE control frame generation including multicast and unicast address
- Automatic detection and checking of PAUSE frames

## Gigabit Ethernet IP with IEEE 1588

### Overview

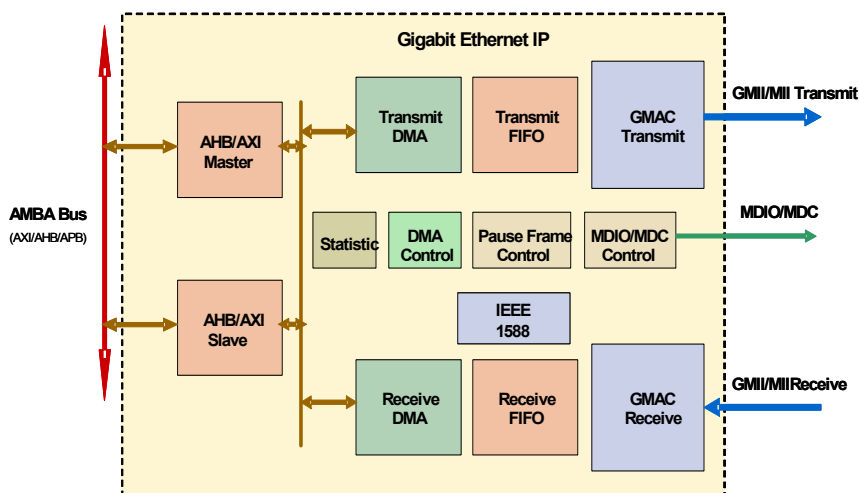
The Arasan Gigabit Ethernet Media Access Controller IP is compliant with the Ethernet IEEE 802.3-2002 standard. The Gigabit Ethernet IP provides a 10/100 Mbps Media Independent Interface (MII) and a 1000 Mbps Gigabit Media Independent Interface (GMII). It also supports optional Reduced MII (RGMII), and Serial GMII (SGMII). The Gigabit Ethernet IP also implements Hardware assisted 1588 Protocol for Timestamping the Receive and Transmit PTP Packets. The Gigabit Ethernet IP is designed for SoC and mobile applications such as integrated networking devices, PCI-Express Ethernet controllers, and Ethernet adapter cards.

The Gigabit Ethernet IP supports half-duplex mode at 10/100 Mbps and full-duplex mode at 10/100/1000 Mbps. The Gigabit Ethernet IP core consists of two configurable FIFOs on both transmit and receive sides to handle the application's latency during frame transmission and reception. A processor bus master and a 32-bit scatter-gather DMA transfer packets between the internal FIFOs and the host memory to enhance system performance.

The Gigabit Ethernet IP supports 4-bit MII based 10/100 Mbps PHY and 8-bit GMII based 10/100/1000 Mbps PHY. A MDIO/MDC (Management Data Input/Output and Management Data Clock) management interface provides control and management functions to external PHY devices.

The Gigabit Ethernet IP also provides enhanced programmable features for minimizing applications complexity and pre/post message processing. The Gigabit Ethernet IP supports MIB, SNMP, RMON, VLAN Q-Tag frame, and Jumbo frames. It also includes dynamic generation, checking, and stripping of FCS field, automatic pad field insertion, automatic retransmission and detection of collision frames, collision avoidance and handling. Other features of the Gigabit Ethernet IP includes generation and decoding of PAUSE control frames, frame boundary delimitation, frame synchronization, and error detection.

Gigabit Ethernet IP Functional Block Diagram



# Gigabit Ethernet IP with IEEE 1588

## GMII/MII Interface:

The GMII and MII interfaces are compliant to the IEEE 802.3-2002 clause 36 and clause 22 respectively. The interfaces can be connected to any standard compliant MII or GMII PHY. Full-duplex mode at 10/100/1000 Mbps and half-duplex mode at 10/100 Mbps are supported. Optional interfaces include RMII, SMII, RGMII, and SGMII.

## Gigabit Ethernet IP Receiver:

The receiver can be programmed to check minimum Inter Frame Gap (IFG) between frames and handles minimum IFG of 64 BT during back to back frame reception. It can also handle reception of frames with no preamble and only SFD. The receiver implement flexible address filtering mode with four 48-bit MAC addresses. A 64-bit hash table is included to filter multicast addresses.

## Gigabit Ethernet IP Transmitter:

The transmitter supports variable length (64 BT, 96 BT, 128 BT, 256 BT) IFG on back to back frame transmission with default value of 128 bit times of IFG. It also supports variable length (3, 5, 7 bytes) preamble generation with default of 7 bytes of preamble. Other features include automatic generation of FCS and PAD during transmission, option to disable PAD and/or CRC32 insertion on transmission on a per frame basis, and option to shield the application for frame retransmission process on collisions during half-duplex mode.

## 1588 Support

The 10/100/1000 Ethernet IP Supports Hardware Assisted 1588 Protocol implementation by extracting System Time value for both receive and Transmit PTP Packets. On transmit, it will timestamp the PTP Packets under software control

## Related Products:

Arasan has a software driver for the Gigabit (10/100/1000 Mbps) Ethernet IP for Windows and Linux OS. To accelerate system design, an Ethernet Hardware Development Kit is available. Arasan also has Fast (10/100 Mbps) Ethernet IP core and a corresponding driver.

and returns the Time Stamp to Software. On Receive, it will parse through the packet and identifies the PTP Packets and if it matches the programmed parameters, will timestamps the packet which is provided to software. Supports both V1 and V2 PTP Packets.

## MDIO/MDC Interface:

The MDIO/MDC interface is a 2-wire interface used to configure and control external IEEE802.3 compliant PHY devices using the MII Management Frame structure. The interface is defined in the IEEE802.3 Specification.

## DMA:

The 32-bit scatter-gather DMA supports either the linked-list or ring (chained) descriptors. The skip length is programmable between descriptors when chained descriptors are used. Up to two buffers per descriptor are supported. The transmit DMA and receive DMA are operating independently. A programmable interrupt structure is used for the DMA. Big or little endian operation is supported.

## Host Interface:

Available host interfaces for the Gigabit Ethernet IP include AXI and AHB. The bus master interface is used to transfer packets between the host memory and the internal FIFOs. The slave interface is used to control the operation of the Ethernet controller and to program the registers inside the core.

## Custom Interface:

The Gigabit Ethernet IP also supports PowerPC, MIPS, SH3/SH4, 8051, and other processor buses. In addition, standard interfaces like PCI and PCIe, and custom bus interface with special requirements can also be implemented.

## Benefits:

- Fully compliant core with proven silicon
- Premier direct support from Arasan IP core designers
- Easy-to-use industry standard test environment
- Un-encrypted source code allows easy implementation
- Reuse Methodology Manual guidelines (RMM) compliant verilog code ensured using Spyglass

## Deliverables:

- RMM Compliant Synthesizable RTL design in Verilog
- Easy-to-use test environment
- Synthesis scripts
- Technical documents

## Supported Platforms/Simulators:

- Platforms: Solaris, Unix, Linux and Win XP
- Verilog simulators: Synopsys VCS, Cadence NC-Verilog, MTI ModelSim-Verilog

## Related Products:

- Ethernet Windows / Linux Driver
- Fast (10/100 Mbps) Ethernet IP
- Ethernet Hardware Development Kit (HDK)

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## Data Sheet Links:

Gigabit Ethernet IP:  
<http://www.arasan.com/datasheets/login.php>

For a complete directory of Arasan IPs, please visit:  
[www.arasan.com](http://www.arasan.com)

