

16550D High Speed UART IP Core

Features

- Complies with UART 16550D specification
- Complies with SD_PHS Specification Ver1.0
- Supports character mode, FIFO mode, and extended FIFO mode
- Maximum 255 bytes FIFO size
- Programmable baud rate generator
- Maximum baud rate up to 1Mb/s
- 5-, 6-, 7-, or 8-bit per character
- 1, 1.5, or 2 stop bits.
- Even, odd, or stick parity
- Interrupt controller
- Complete status reporting

Overview

The Arasan 16550D High Speed UART IP core is a 16550-compliant Universal Asynchronous Receiver/Transmitter (UART) with FIFO or expanded FIFO. The UART performs serial to parallel conversion of data received from the serial interface, and parallel to serial conversion of data received from the CPU interface. Both character and FIFO modes are supported.

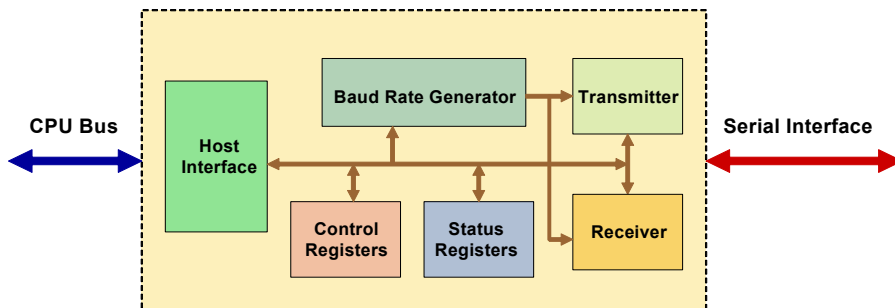
Operation of the UART can be programmed by a host processor through the host interface. Writing to the Control register determines the operational mode of the UART. The transmitter and receiver at the serial interface perform parallel to serial and serial to parallel conversion of data.

Baud rate clock and receiver reference clock are generated by the Baud Rate Generator. Writing to the Divisor Latch Registers (DLL & DLM) controls the clock rate. The interrupt controller signals the host processor in the event of error conditions such as transmission errors or modem status changes

Complete status of the UART can be accessed by the host processor at any time. The Status registers provide information such as the modem status, line condition, line break, overrun, parity error, and other conditions.

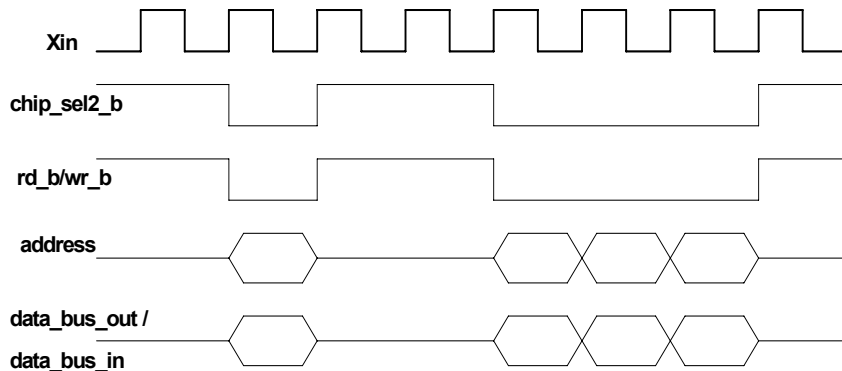
The 16550D High Speed UART IP core is an RTL design in Verilog and VHDL that implements an UART on an ASIC, or FPGA. The core includes RTL code, test scripts and a test environment for full simulation verifications. The Arasan 16550D High Speed UART IP core has been widely used in different applications by major chip vendors.

16550D High Speed UART IP Core Functional Block Diagram

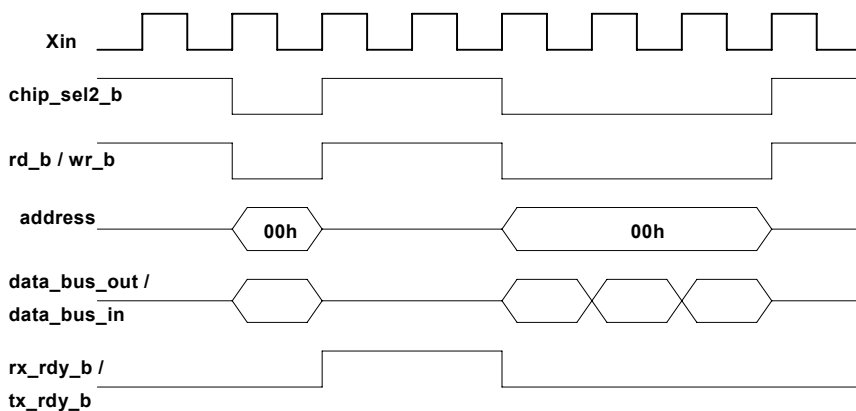


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Register read/write timing diagram



Data read/write timing diagram



Benefits:

- Fully compliant core with proven silicon
- Premier direct support from Arasan IP core designers
- Easy-to-use industry standard test environment
- Unencrypted source code allows easy implementation
- ReUse Methodology Manual guidelines (RMM) compliant Verilog code ensured using Spyglass

Deliverables:

- RMM Compliant Synthesizable RTL design in Verilog
- Easy-to-use test environment
- Synthesis scripts
- Technical documents

Supported Platforms/Simulators:

- Platforms: Solaris, Unix, Linux and Win XP
- Verilog simulators: Synopsys VCS, Cadence NC-Verilog, MTI ModelSim-Verilog

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Data Sheet Links:

16550D High Speed UART IP core:
<http://www.arasan.com/datasheets/login.php>

For a complete directory of Arasan IPs, please visit:
www.arasan.com

